

DESIGN OF OPTIMAL NANOSCALE
CHANNEL DIMENSIONS OF FINFET BASED
ON CONSTITUENT SEMICONDUCTOR
MATERIALS

AHMED MAHMOOD ALI

MASTER OF SCIENCE

UNIVERSITI MALAYSIA PAHANG



SUPERVISOR'S DECLARATION

We hereby declare that we have checked this thesis and in our opinion, this thesis is adequate in terms of scope and quality for the award of the degree of Master of Science.

(Supervisor's Signature)

Full Name : DR. WAHEB ABDUL JABBAR SHAIK ABDULLAH

Position : SENIOR LECTURER

Date :

(Co-supervisor's Signature)

Full Name : DR. HADI BIN MANAP

Position : ASSOCIATE PROFESSOR

Date :



STUDENT'S DECLARATION

I hereby declare that the work in this thesis is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at Universiti Malaysia Pahang or any other institutions.

(Student's Signature)

Full Name : AHMED MAHMOOD ALI

ID Number : MEL 17006

Date :

DESIGN OF OPTIMAL NANOSCALE CHANNEL DIMENSIONS OF FINFET
BASED ON CONSTITUENT SEMICONDUCTOR MATERIALS

AHMED MAHMOOD ALI

Thesis submitted in fulfilment of the requirements
for the award of the degree of
Master of Science

Faculty of Engineering Technology
UNIVERSITI MALAYSIA PAHANG

MAY 2019

ACKNOWLEDGMENTS

In the name of God, the Merciful praise is to God and prayers and peace on our master and our beloved Muhammad the Messenger of Allah (may Allah bless him and grant him peace) and his honourable companions and those who followed for him. Thanks to God for his grace these studies have been conducted successfully. I would like to express my appreciation and special thanks to my supervisors Dr. Waheb Abdul Jabbar Al-Areeqi, my co-supervisor, Dr. Hadi Bin Manap, and my ex-supervisor Dr. Yasir Hashim. They have always been happy and willing to help me and direct me to the outcome of the thesis. I am grateful to Universiti Malaysia Pahang (UMP). Thanks also for the FTeK staff for their help. Finally, my regards and blessings go to my family. Words cannot express my gratitude to my parents for all the sacrifices made on my behalf. Special thanks to my wives who sacrificed in order to reach my goal. I would also like to thank all my friends who supported me and encouraged me to pursue my goal. Thank you all and God bless.

ABSTRAK

Aplikasi Nanoelectronic telah mendapat manfaat yang sangat besar daripada kemajuan besar dalam industri teknologi Nano yang baru muncul. Penurunan nilai yang besar dari dimensi transistor telah membolehkan penempatan lebih dari 100 juta transistor pada satu cip sekali gus mengurangkan fungsi peningkatan kos dan prestasi litar bersepadu (IC) yang dipertingkatkan. Walau bagaimanapun, kajian untuk mengurangkan saiz transistor konvensional akan menjadi sanjatan mencabar kerana kebocoran elektrostatik dan isu fabrikasi lain. Fin Field Effect Transistor (FinFET) menunjukkan potensi besar dalam penskalaan saiz dan pembuatan sebagai calon yang menjanjikan teknologi nano-oksida-semikonduktor (CMOS) pelengkap nanoscale. Struktur FinFET menyediakan kawalan elektrik yang lebih baik ke atas konduksi saluran dengan itu ia telah menarik minat yang luas dari para penyelidik dalam kedua-dua akademik dan industri. Walau bagaimanapun, ia secara agresif menurunkan dimensi saluran terutamanya panjang saluran akan menurunkan prestasi keseluruhan akibat kesan saluran pendek yang merugikan (SCEs). Tujuan kajian ini adalah untuk mengkaji dan menganalisis ciri-ciri elektrik pelbagai jenis transistor FinFET (Si, GaAs, Ge dan InAs) berdasarkan dimensi saluran untuk mengenal pasti had pengukuran fizikal optimum untuk prestasi transistor terbaik. Kajian komparatif berasaskan simulasi TIGAs (3) parameter berubah-ubah: lebar panjang dan ketebalan oksida saluran dijalankan. Kesan mengubah dimensi saluran pada prestasi setiap jenis FinFET dinilai berdasarkan EMPAT (4) ciri elektrik iaitu; (i) Nisbah I_{ON} / I_{OFF} (ii) Tegangan Ambang Swing (SS) (V_T) dan Pengurangan Barrier-induced Drain (DIBL). Alat simulasi MuGFET yang terkenal untuk struktur FET pelbagai pintu gerbang nano digunakan untuk menjalankan simulasi percubaan di bawah syarat-syarat yang dipertimbangkan. Dimensi saluran optimum untuk prestasi terbaik dari semua jenis FinFET yang dipertimbangkan telah dicapai pada faktor skala minimum $K = 0.125$. Selain itu Si-FinFET mengatasi GaAs-FinFET dan kedua-duanya mengekalkan prestasi unggul dari segi nisbah I_{ON} / I_{OFF} dan nilai SS berbanding dengan dua jenis FinFET yang lain. Sebaliknya prestasi Ge-FinFET telah direndahkan dan mencapai nisbah I_{ON} / I_{OFF} paling rendah manakala ciri-ciri terburuk dari segi nilai SS (94 mV / dec) telah berlaku pada InAs-FinFET. Hasil penyelidikan menyumbang ke arah menganalisa had skala dan dimensi saluran penurunan tahap FinFET sebagai pengganti berpotensi untuk transistor planar dan memahaminya lagi prestasi mereka untuk mengurangkan kebocoran semasa dan masalah SCE lain.

ABSTRACT

Nano-electronic applications have benefited enormously from the great advancement in the emerging Nano-technology industry. The tremendous downscaling of the transistors' dimensions has enabled the placement of over 100 million transistors on a single chip thus reduced cost, increased functionality and enhanced performance of integrated circuits (ICs). However, reducing size of the conventional planar transistors would be exceptionally challenging due to leakages electrostatics and other fabrication issues. Fin Field Effect Transistor (FinFET) shows a great potential in scalability and manufacturability as a promising candidate in nanoscale complementary metal-oxide-semiconductor (CMOS) technologies. The structure of FinFET provides superior electrical control over the channel conduction, thus it has attracted widespread interest from researchers in both academia and industry. However, aggressively scaling down of channel dimensions, mainly the channel length, will degrade the overall performance due to detrimental short channel effects (SCEs). The aim of this study is to design optimal Nano-dimensional channel of FinFET based on electrical characteristics and semiconductor material (Si GaAs Ge and InAs) to overcome dimensions shrunk down issues and ensure the best performance of FinFETs. This was achieved by proposing a new scaling factor, K , to simultaneously shrinking the physical scaling limits of channel dimensions for various FinFETs without degrading their performance. A simulation-based comprehensive comparative study depending on FOUR (4) variable parameters: length, width and oxide thickness of channel in addition to scaling factor were carried out. The impact of changing channel dimensions on the performance of each type of FinFETs was evaluated base on FOUR (4) electrical characteristics namely; (i) I_{ON}/I_{OFF} ratio (ii) Subthreshold Swing (SS), (iii) Threshold voltage (V_T), and (iv) Drain-induced barrier lowering (DIBL). The well-known MuGFET simulation tool for nano-scale multi-gate FET structure is utilized to conduct experimental simulations under the considered conditions. The obtained simulation results showed that the optimal channel dimensions for best performance of all considered FinFETs types were achieved at a minimal scaling factor $K = 0.125$ with 5 nm length, 2.5 nm width and 0.625 nm oxide thickness of channel. Furthermore, Si-FinFET achieved the highest I_{ON}/I_{OFF} ratio (up to 2.12×10^8) and outperformed GaAs-FinFET, and both maintained a superior performance in terms of I_{ON}/I_{OFF} ratio and SS value compared to the other two types of FinFETs. In contrast, the Ge-FinFET performance was degraded and reached the lowest I_{ON}/I_{OFF} ratio (2.29×10^5), whereas the worst characteristics in terms of SS value (94 mV/dec) occurred with InAs-FinFET. The obtained results introduced new limits with enhancing FinFETs performance in terms of the investigated characteristics. The outcomes of this research contribute towards new channel nano scaling limits of FinFETs as potential successors to planar transistors in nanoscale devices and nanotechnology applications, and further analysing the electrical characteristics of FinFETs with reducing leakage current and overcoming SCEs.

TABLE OF CONTENT

TITLE PAGE	
ACKNOWLEDGMENTS	ii
ABSTRAK	iii
ABSTRACT	iv
TABLE OF CONTENT	v
LIST OF TABLES	ix
LIST OF FIGURES	x
LIST OF SYMBOLS	xiii
LIST OF ABBREVIATIONS	xiv
 CHAPTER 1 INTRODUCTION	 1
1.1 Background of Study	1
1.2 Problem Statement	5
1.3 Research Objectives	7
1.4 Scope of Study	7
1.5 Thesis Organisation	8
 CHAPTER 2 LITERATURE REVIEW	 9
2.1 Introduction	9
2.2 Overview of Nanotechnology and its Future Implications	9
2.3 The Field-Effect Transistor	11
2.3.1 Types of the Field-effect Transistor	12

2.3.2	The Metal-Oxide-Semiconductor-Field-Effect-Transistor	13
2.3.3	The Short Channel Effects	15
2.4	Fin Field Effect Transistor	16
2.5	Moore Law and Scaling of Transistors	20
2.5.1	MOSFET Scaling Down and its Limitations	21
2.5.2	The Scaling Down of FinFET	22
2.6	Electrical Properties of Transistor	28
2.6.1	Sub-threshold Swing	29
2.6.2	ON-to-OFF Current Ratio	29
2.6.3	Threshold Voltage	29
2.6.4	Drain-Induced Barrier Lowering	30
2.7	Semiconductor Materials	30
2.7.1	Silicon Semiconductor	30
2.7.2	Germanium Semiconductor	32
2.7.3	Indium Arsenide Semiconductor	32
2.7.4	Gallium Arsenide	33
2.8	The Effect of Semiconductor Materials on the Electrical Properties of Transistors	34
2.9	Comparative Summary of Previous Studies	36
2.10	Summary	42
CHAPTER 3 METHODOLOGY		43
3.1	Introduction	43
3.2	General Research Methodology	43
3.3	Simulation Tools	44
3.4	Simulation Design	47
3.4.1	Selection of Semiconductor Material	47

3.5	Selection of Channel Dimensions	49
3.5.1	Channel Length Scenario	49
3.5.2	Channel Width Scenario	50
3.5.3	Oxide Thickness Scenario	50
3.5.4	Scaling Factor Scenario	51
3.5.5	The I-V Characteristics	51
3.6	Summary	53
CHAPTER 4 RESULTS AND DISCUSSION		54
4.1	Introduction	54
4.2	The Si-FinFET Scenarios	54
4.2.1	Effect of Varying Channel Length	55
4.2.2	Effect of Varying Channel Width	57
4.2.3	Effect of Varying Channel Oxide Thickness	59
4.2.4	Effect of Varying Scaling Factor of Channel Dimensions	61
4.3	The GaAs-FinFET Scenarios	64
4.3.1	Effect of Varying Channel Length	64
4.3.2	Effect of Varying Channel Width	66
4.3.3	Effect of Varying Channel Oxide Thickness	68
4.3.4	Effect of Varying Scaling Factor of Channel Dimensions	69
4.4	The Ge-FinFET Scenarios	72
4.4.1	Effect of Varying Channel Length	72
4.4.2	Effect of Varying Channel Width	75
4.4.3	Effect of Varying Channel Oxide Thickness	76
4.4.4	Effect of Varying Scaling Factor of Channel Dimensions	79
4.5	The InAs-FinFET Scenarios	81

4.5.1	Effect of Varying Channel Length	82
4.5.2	Effect of Varying Channel Width	85
4.5.3	Effect of Varying Channel Oxide Thickness	86
4.5.4	Effect of Varying Scaling Factor of Channel Dimensions	88
4.6	Comparison of FinFETs Constituent Semiconductor Materials	90
4.7	Summary	95
CHAPTER 5 CONCLUSION		96
5.1	Introduction	96
5.2	Conclusion	96
5.3	Significance of the Study	97
5.4	Recommendations for Future Work	97
REFERENCES		99

LIST OF TABLES

Table 2.1	The nm technologies advancements in the last years	21
Table 2.2	Intel Technology Roadmap	27
Table 2.3	Basic electrical properties of Si-Ge and III-V compounds	36
Table 2.4	Summary of previous studies main finding	41
Table 3.1	Simulation Parameters	47
Table 3.2	The parameter used with condition scaling factor K. of Si-FinFET	51
Table 4.1	List of Simulation Parameters	55
Table 4.2	The parameter used with condition scaling factor K. of Si-FinFET	61
Table 4.3	Summary of Si-FinFET main findings	63
Table 4.4	Simulation Parameters	64
Table 4.5	The parameter used with condition scaling factor K. of GaAs-FinFET	69
Table 4.6	Summary of GaAs-FinFET main findings	71
Table 4.7	The simulation parameters	72
Table 4.8	Channel dimensions based on scaling factor K	79
Table 4.9	Summary of Ge-FinFET main findings	81
Table 4.10	Simulation parameters	82
Table 4.11	Channel dimensions based on scaling factor K	88
Table 4.12	Channel summary of main findings for InAs-FinFET	90
Table 4.13	Overall comparison of semiconductors channel type FinFET	94

LIST OF FIGURES

Figure 1.1	Nanomedicine in cancer therapy laser	2
Figure 1.2	The field effect transistor family tree	3
Figure 1.3	(a) 2-D planar transistor MOSFET (b)3-D Tri-Gate transistor FinFET structure	4
Figure 1.4	Industry Scaling Trend Over the Year	4
Figure 1.5	Power Dissipation with Technology Scales over years	5
Figure 2.1	Timeline History of Nanotechnology	10
Figure 2.2	Application of Nano-electronics	11
Figure 2.3	Cross-section of an n-type MOSFET	12
Figure 2.4	The Evolution of the FET Architecture	14
Figure 2.5	Improvements from planar MOSFET to GAA FET	15
Figure 2.6	Cross-sectional schematics of (a) DELTA transistor (b) FinFET transistor	16
Figure 2.7	(a) 2-D planar transistor (b)3-D Tri-Gate transistor FinFET structure	18
Figure 2.8	(a) Planar transistor (b) A 3D FinFET (tri-gate) (c) 3D FinFET with three fins	19
Figure 2.9	Enhanced electrical characteristics of FinFET by laser annealing	20
Figure 2.10	(a) planar transistor (b) FinFET transistor	22
Figure 2.11	The 22 nm Tri-GATe Transistor	23
Figure 2.12	Transistor Gate Delay active power can be more than 50% compared to its 32 nm process	24
Figure 2.13	Transistor gate delay increase in performance vs operating voltage	25
Figure 2.14	Twice fitting of many transistors in the same die area at 22 nm	25
Figure 2.15	Tri-Gate Transistor Benefits	26
Figure 2.16	(a) First generation FinFET at 22 nm node -2011 (b) Second generation FinFET at 14 nm node- 2013 (c) Third generation FinFET at 10-nm node-2017	27
Figure 2.17	Semiconductors manufacture pressers	28
Figure 2.18	Purified crystalline silicon with a diamond cubic crystal structure	31
Figure 2.19	Grayish lustrous block with an uneven cleaved surface	32
Figure 2.20	Sphalerite-unit-cell-3D-balls with Indium arsenide crystals	33
Figure 2.21	GaAs can be used for various transistor types	34
Figure 2.22	CPU power density trend in the last decade	35
Figure 3.1	Flow chart of research methodology	45

Figure 3.2	The “MuGFET ” simulation tool homepage	46
Figure 3.3	Parameter selection	48
Figure 3.4	Selection of silicon parameters as a semiconductor in simulation	48
Figure 3.5	Voltage gate and temperature options	49
Figure 3.6	The channel length selection	50
Figure 3.7	Selection of channel width and oxide thickness	51
Figure 3.8	Selection of electrical characteristics from the ‘simulate’ option	52
Figure 3.9	Selection of the electrical characteristic type	52
Figure 3.10	Description of how to extract and draw electrical properties with changing length (20 to 100) nm in FinFET and Nanowire.	53
Figure 4.1	ION/IOFF ratio with a channel length of Si-FinFET	56
Figure 4.2	SS with a channel length of Si-FinFET	56
Figure 4.3	VT and DIBL with a channel length of Si-FinFET.	57
Figure 4.4	ION/IOFF with a channel width of Si-FinFET	58
Figure 4.5	SS with a channel width of Si-FinFET	58
Figure 4.6	VT, DIBL with a channel width of Si-FinFET	59
Figure 4.7	ION/IOFF with an oxide thickness of Si-FinFET	59
Figure 4.8	SS with an oxide thickness of Si-FinFET	60
Figure 4.9	VT and DIBL with channel oxide thickness of Si-FinFET	61
Figure 4.10	ION/IOFF with scaling factor of Si-FinFET	62
Figure 4.11	SS with scaling factor (K) of Si-FinFET	62
Figure 4.12	VT and DIBL with scaling factor of Si-FinFET	63
Figure 4.13	ION/IOFF with a channel length of GaAs-FinFET	65
Figure 4.14	SS with a channel length of GaAs-FinFET	65
Figure 4.15	VT and DIBL with a channel length of GaAs-FinFET	66
Figure 4.16	ION/IOFF with a channel width of GaAs-FinFET	66
Figure 4.17	SS with a channel width of GaAs-FinFET	67
Figure 4.18	VT and DIBL with a channel width of GaAs-FinFET	67
Figure 4.19	ION/IOFF with an oxide thickness of GaAs-FinFET	68
Figure 4.20	SS with an oxide thickness of GaAs-FinFET	68
Figure 4.21	VT and DIBL with channel oxide thickness of GaAs-FinFET	69
Figure 4.22	ION/IOFF with scaling factor of GaAs-FinFET	70
Figure 4.23	SS with scaling factor of GaAs-FinFET	70
Figure 4.24	VT and DIBL with scaling factor of GaAs-FinFET	71

Figure 4.25	ION/IOFF with a channel length of Ge-FinFET	73
Figure 4.26	SS with a channel length of Ge-FinFET	74
Figure 4.27	VT and DIBL with a channel length of Ge-FinFET	74
Figure 4.28	ION/IOFF with a channel width of Ge-FinFET	75
Figure 4.29	SS with a channel width of Ge-FinFET	76
Figure 4.30	VT and DIBL with a channel width of Ge-FinFET	76
Figure 4.31	ION/IOFF with an oxide thickness of Ge-FinFET	77
Figure 4.32	SS with an oxide thickness of Ge-FinFET	78
Figure 4.33	VT -DIBL with channel oxide thickness of Ge-FinFET	78
Figure 4.34	ION/IOFF with scaling factor of Ge-FinFET	80
Figure 4.35	SS with scaling factor of Ge-FinFET	80
Figure 4.36	VT and DIBL with scaling factor of Ge-FinFET	81
Figure 4.37	ION/IOFF with a channel length of InAs-FinFET	83
Figure 4.38	SS with a channel length of InAs-FinFET	84
Figure 4.39	VT and DIBL with a channel length of InAs-FinFET	84
Figure 4.40	ION/IOFF with a channel width of InAs-FinFET	85
Figure 4.41	SS with a channel width of InAs-FinFET	86
Figure 4.42	VT and DIBL with a channel width of InAs-FinFET	86
Figure 4.43	ION/IOFF with an oxide thickness of InAs-FinFET	87
Figure 4.44	SS with an oxide thickness of InAs-FinFET	87
Figure 4.45	VT and DIBL with channel oxide thickness of InAs-FinFET	88
Figure 4.46	ION/IOFF with scaling factor of InAs-FinFET	89
Figure 4.47	SS with scaling factor of InAs-FinFET	89
Figure 4.48	VT and DIBL with scaling factor of InAs-FinFET	90
Figure 4.49	ION/IOFF vs. K for different semiconductors of FinFET	91
Figure 4.50	SS vs. K for different semiconductors of FinFET	92
Figure 4.51	VT vs. K at different semiconductors of FinFET	93
Figure 4.52	DIBL vs. K for different semiconductors of FinFET	93

LIST OF SYMBOLS

D	Drain
DIBL	Drain induced barrier lowering
I	current
I_d	Drain current
I_{OFF}	OFF Current
I_{ON}	ON current
K	Scaling factor
K_B	Boltzmann's coefficient
L	Length of the channel
Q	Electron charge
R_{OUT}	Output resistance
S	Source
SS	Subthreshold Swing
T	Temperature
T_{OX}	Oxide thickness
V	Voltage
V_d	Drain voltage
V_{DD}	Drain DC voltage source
V_{DS}	Drain to source voltage
V_{GS}	Gate to source voltage
V_T	Threshold voltage
W	Width of the channel

LIST OF ABBREVIATIONS

CPU	Unit processing of the central
DELTA	Depleted lean channel transistor
FDSOI	Full-Depleted Silicon
FDSOI	Depleted Silicon On Insulator
FET	Field Effect Transistor
FinFET	Fin-shaped field effect transistor
GAA	Gate all around
GaAs	Gallium Arsenide
GaN	Gallium Nitride
Ge	Germanium
GIDL	Gate-induced drain leakage
IC	Integrated Circuits
InAs	Indium Arsenide
JFETs	Junction field effect transistor
MOSFET	Metal-Oxide-field-effect transistor
MuGFET	Multi-Gate-Field Effect Transistor
NW	Nanowire
PDSOI	Partially-Depleted Silicon
Rsd	Resistance source drain
SCE	Short channel effect
Si	Silicon
SiC	Silicon Carbide
SiNWT	Silicon nanowire transistor
SOI	Silicon on insulator
VLST-TSA	Technology Systems and Application

REFERENCES

- Angelo, R. M., Brown, A. S., Wolter, S., & Lampert, W. V. (2018). Sensors incorporating antibodies and methods of making and using the same: Google Patents.
- Arora, N. D. (2012). *MOSFET models for VLSI circuit simulation: theory and practice*: Springer Science & Business Media.
- Asadollahi, A. (2018). *Fabrication of Group IV Semiconductors on Insulator for Monolithic 3D Integration*. Kungliga Tekniska högskolan.
- Becker, R., & Ossig, M. (2013). Device for optically scanning and measuring an environment: Google Patents.
- Bikki, P., & Karuppanan, P. (2017). SRAM Cell Leakage Control Techniques for Ultra Low Power Application: A Survey. *Circuits and Systems*, 8(02), 23.
- Bohr, M. (2014). *14 nm process technology: Opening new horizons*. Paper presented at the Intel Developer Forum.
- Bohr, M., & Mistry, K. (2011). Intel's revolutionary 22 nm transistor technology. *Intel website*.
- Bohr, M. T., & Young, I. A. (2017). CMOS scaling trends and beyond. *IEEE Micro*, 37(6), 20-29.
- Bouville, F., Maire, E., Meille, S., Van de Moortèle, B., Stevenson, A. J., & Deville, S. (2014). Strong, tough and stiff bioinspired ceramics from brittle constituents. *Nature materials*, 13(5), 508.
- Brock, D. C., & Moore, G. E. (2006). *Understanding Moore's law: four decades of innovation*: Chemical Heritage Foundation.
- Cai, B., Wang, S., Huang, L., Ning, Y., Zhang, Z., & Zhang, G.-J. (2014). Ultrasensitive label-free detection of PNA–DNA hybridization by reduced graphene oxide field-effect transistor biosensor. *ACS nano*, 8(3), 2632-2638.
- Cherupalli, H., Duwe, H., Ye, W., Kumar, R., & Sartori, J. (2017). *Bespoke processors for applications with ultra-low area and power constraints*. Paper presented at the Computer Architecture (ISCA), 2017 ACM/IEEE 44th Annual International Symposium on.
- Choi, Y.-K., King, T.-J., & Hu, C. (2002). Nanoscale CMOS spacer FinFET for the terabit era. *IEEE Electron Device Letters*, 23(1), 25-27.
- Chugh, C. (2018). *The Effects of Variation in Geometry Parameters on Sub-50 nm Finfet and Their Direct Impact on Finfet Performance*. Paper presented at the 2018 International Conference on Intelligent Circuits and Systems (ICICS).

- Chun, B.-G., Ihm, S., Maniatis, P., Naik, M., & Patti, A. (2011). *Clonecloud: elastic execution between mobile device and cloud*. Paper presented at the Proceedings of the sixth conference on Computer systems.
- Colinge, J.-P., Lee, C.-W., Afzalian, A., Akhavan, N. D., Yan, R., Ferain, I., White, M. (2010). Nanowire transistors without junctions. *Nature nanotechnology*, 5(3), 225.
- Das, R., & Baishya, S. (2018). Dual-material gate dual-stacked gate dielectrics gate-source overlap tri-gate germanium FinFET: analysis and application. *Indian Journal of Physics*, 1-9.
- Dennard, R. H., Cai, J., & Kumar, A. (2018). A perspective on today's scaling challenges and possible future directions *Handbook of Thin Film Deposition (Fourth Edition)* (3-18): Elsevier.
- Dong, J., Li, H., & Li, L. (2013). Multi-functional nano-electronics constructed using boron phosphide and silicon carbide nanoribbons. *NPG Asia Materials*, 5(7), e56.
- Duriez, B., Vellianitis, G., Van Dal, M., Doornbos, G., Oxland, R., Bhuwanka, K., . . . Yin, K. (2013). *Scaled p-channel Ge FinFET with optimized gate stack and record performance integrated on 300mm Si wafers*. Paper presented at the Electron Devices Meeting (IEDM), 2013 IEEE International.
- Ferrari, A. C., Bonaccorso, F., Fal'Ko, V., Novoselov, K. S., Roche, S., Bøggild, P., Pugno, N. (2015). Science and technology roadmap for graphene, related two-dimensional crystals, and hybrid systems. *Nanoscale*, 7(11), 4598-4810.
- Fiori, G., Bonaccorso, F., Iannaccone, G., Palacios, T., Neumaier, D., Seabaugh, A., Colombo, L. (2014). Electronics based on two-dimensional materials. *Nature nanotechnology*, 9(10), 768.
- Flamm, K. (2018). *Measuring Moore's Law: Evidence from Price, Cost, and Quality Indexes*.
- Furber, S. B. (2017). *VLSI RISC architecture and organization*: Routledge.
- Gandhi, R., Chen, Z., Singh, N., Banerjee, K., & Lee, S. (2011). Vertical Si-Nanowire n p -Type Tunneling FETs With Low Subthreshold Swing (≤ 50 mV/decade) at Room Temperature. *IEEE Electron Device Letters*, 32(4), 437-439.
- Gardea-Torresdey, J. L., Rico, C. M., & White, J. C. (2014). Trophic transfer, transformation, and impact of engineered nanomaterials in terrestrial environments. *Environmental science & technology*, 48(5), 2526-2540.
- Geological, S. (2008). Germanium—statistics and information. *US Geological Survey. Mineral Commodity Summaries*.

- Ghoneim, M. T., & Hussain, M. M. (2015). Review on physically flexible nonvolatile memory for internet of everything electronics. *Electronics*, 4(3), 424-479.
- Goettler, R. L., & Gordon, B. R. (2011). Does AMD spur Intel to innovate more? *Journal of Political Economy*, 119(6), 1141-1200.
- Haider, F., Chee, F., Abu Hassan, H., & Saafie, S. (2017). *Monte Carlo simulation to calculate the rate of ^{137}Cs gamma rays dispersion in gallium arsenide compound*. Paper presented at the AIP Conference Proceedings.
- Hajare, R., Lakshminarayana, C., GH, C. P. R., & Hegde, Y. (2015). *Performance evaluation of FinFET and Nanowire at different technology nodes*. Paper presented at the Emerging Research in Electronics, Computer Science and Technology (ICERECT), 2015 International Conference .
- Hammarlund, P., Martinez, A. J., Bajwa, A. A., Hill, D. L., Hallnor, E., Jiang, H., . . . Kumar, R. (2014). Haswell: The fourth-generation intel core processor. *IEEE Micro*, 34(2), 6-20.
- Harikrishnan, R. (2018). Amalgamating Nanoscience with Robotics Technology to Influence the Behaviour of Fractal Robots: A Focus on Future Applications.
- Hashim, Y. (2017). *Investigation of FinFET as a Temperature Nano-Sensor Based on Channel Semiconductor Type*. Paper presented at the IOP Conference Series: Materials Science and Engineering.
- Hey, A. (2018). *Feynman and computation*: CRC Press.
- Ionescu, A. M. (2010). Electronic devices: nanowire transistors made easy. *Nature nanotechnology*, 5(3), 178.
- Issa, H. A. (2016). *Mehano-hemijski i termički tretman železonosnih otpadnih materijala: ekološki doprinosi i sinergetski efekti (Mechano-chemical and thermal treatment of iron bearing waste materials: ecological benefits and synergetic effects)*. Univerzitet u Beogradu-Tehnološko-metalurški fakultet.
- Jorgenson, D. W., Ho, M. S., & Samuels, J. D. (2014). *Long-term estimates of US productivity and growth*. Paper presented at the Prepared for Presentation at the Third World KLEMS Conference: Growth and Stagnation in the World Economy.
- Kaundal, S., & Rana, A. K. (2018). Physical Insights on Scaling of Gaussian Channel Design Junctionless FinFET. *Journal of Nanoelectronics and Optoelectronics*, 13(5), 653-660.
- Keyser, U. F. (2016). Enhancing nanopore sensing with DNA nanotechnology. *Nature nanotechnology*, 11(2), 106.

- Khan, F. S., Anwer, R. M., Van de Weijer, J., Bagdanov, A. D., Vanrell, M., & Lopez, A. M. (2012). *Color attributes for object detection*. Paper presented at the Computer Vision and Pattern Recognition (CVPR), 2012 IEEE Conference.
- Khan, W., & Pop, I. (2010). Boundary-layer flow of a nanofluid past a stretching sheet. *International journal of heat and mass transfer*, 53(11-12), 2477-2483.
- Kimura, H., Atsumi, T., & Yamazaki, S. (2018). Semiconductor device and electronic device: Google Patents.
- Mack, C. (2015). The multiple lives of Moore's law. *IEEE Spectrum*, 52(4), 31-31.
- Meija, J., Coplen, T. B., Berglund, M., Brand, W. A., De Bièvre, P., Gröning, M., Walczyk, T. (2016). Atomic weights of the elements 2013 (IUPAC Technical Report). *Pure and Applied Chemistry*, 88(3), 265-291.
- Mistry, K. (2017). 10 nm technology leadership. *Intel, Technology and Manufacturing Day Presentation*.
- Mobarakeh, M. S., Omrani, S., Vali, M., Bayani, A., & Omrani, N. (2018). Theoretical logic performance estimation of Silicon, Germanium and SiGe Nanowire Fin-field effect transistor. *Superlattices and Microstructures*.
- Murray, C. J., Abraham, J., Ali, M. K., Alvarado, M., Atkinson, C., Baddour, L. M., . . . Birbeck, G. (2013). The state of US health, 1990-2010: burden of diseases, injuries, and risk factors. *Jama*, 310(6), 591-606.
- Nagy, D., Indalecio, G., García-Loureiro, A. J., Elmessary, M. A., Kalna, K., & Seoane, N. (2018). FinFET Versus Gate-All-Around Nanowire FET: Performance, Scaling, and Variability. *IEEE Journal of the Electron Devices Society*, 6(1), 332-340.
- Niccolai, J. (2015). Intel pushes 10nm chip-making process to 2017, slowing Moore's Law. *InfoWorld*.
- Peng, J., Qi, Y., Lo, H.-C., Zhao, P., Yong, C., Yan, J., . . . Regonda, S. (2017). Source/drain eSiGe engineering for FinFET technology. *Semiconductor Science and Technology*, 32(9), 094004.
- Pop, E. (2010). Energy dissipation and transport in nanoscale devices. *Nano Research*, 3(3), 147-169.
- Pradhan, K. P., & Sahu, K. P. (2016). Benefits of asymmetric underlap dual-k spacer hybrid fin field-effect transistor over bulk fin field-effect transistor. *IET Circuits, Devices & Systems*, 10(5), 441-447.
- Quinn, R., Andriamanalimanana, B. R., Sengupta, S., & Spetka, S. (2018). *Applicability of the Julia Programming Language to Forward Error-Correction Coding in Digital Communications Systems*.

- Rana, P. (2017). *Electrostatic Analysis of Gate All Around (GAA) Nanowire over FinFET*. Arizona State University.
- Richerson, D. W., & Lee, W. E. (2018). *Modern ceramic engineering: properties, processing, and use in design*: CRC press.
- Rowell, R. M. (2012). *Handbook of wood chemistry and wood composites*: CRC press.
- Ruan, D.-B., Chang-Liao, K.-S., Li, Y.-L., Feng, H.-T., Hsu, Y.-W., Huang, C.-H., Yang, M.-Y. (2017). Enhanced electrical characteristics of FinFET by rapid-thermal-and-laser annealing with suitable power. *Microelectronic Engineering*, 178, 56-60.
- Ruzyllo, J. (2016). *Semiconductor Glossary: A Resource for Semiconductor Community*: World Scientific.
- Sakakibara, J., Noda, Y., Shibata, T., Nogami, S., Yamaoka, T., & Yamaguchi, H. (2008). *600V-class super junction MOSFET with high aspect ratio P/N columns structure*. Paper presented at the 2008 20th International Symposium on Power Semiconductor Devices and IC's.
- Sankey, T., Donager, J., McVay, J., & Sankey, J. B. (2017). UAV lidar and hyperspectral fusion for forest monitoring in the southwestern USA. *Remote Sensing of Environment*, 195, 30-43.
- Schwierz, F. (2010). Graphene transistors. *Nature nanotechnology*, 5(7), 487.
- Seoane, N., Indalecio, G., Nagy, D., Kalna, K., & García-Loureiro, A. J. (2018). Impact of Cross-Sectional Shape on 10-nm Gate Length InGaAs FinFET Performance and Variability. *IEEE Transactions on Electron Devices*, 65(2), 456-462.
- Shen, M.-Y. (2017). *Effect of Ion Flux (Dose Rate) in Source-Drain Extension Ion Implantation for 10-nm Node FinFET and Beyond on 300/450mm Platforms*: State University of New York at Albany.
- Shenai, K., Scott, R. S., & Baliga, B. J. (1989). Optimum semiconductors for high-power electronics. *IEEE Transactions on Electron Devices*, 36(9), 1811-1823.
- Snodgrass, E. M., Checca, M., Norman, S. C., & Reynolds, T. K. (2013). Ensuring that US Engineers Remain Globally Competitive.
- Sousa, M. A., Esteves, T. C., Sedrine, N. B., Rodrigues, J., Lourenço, M. B., Redondo-Cubero, A., . . . Wetzol, C. (2015). Luminescence studies on green emitting InGaN/GaN MQWs implanted with nitrogen. *Scientific reports*, 5, 9703.
- Sriramkumar, V., Paydavosi, N., Duarte, J., Lu, D., Lin, C.-H., Dunga, M., Hu, C. (2013). BSIM-CMG 107.0. 0 Multi-Gate MOSFET Compact Model. *Technical Manual*.

- Taylor, M. B. (2012). *Is dark silicon useful? Harnessing the four horsemen of the coming dark silicon apocalypse*. Paper presented at the Design Automation Conference (DAC), 2012 49th ACM/EDAC/IEEE.
- Tian, J. (2017). *Theory, Modelling and Implementation of Graphene Field-Effect Transistor*. Queen Mary University of London.
- Uddin, M. N., Emon, B., & Ullah, A. (2015). Simulation & Analysis of Characteristics of tunnel FET: Northern University Bangladesh, Dhaka.
- Van Dal, M., Vellianitis, G., Doornbos, G., Duriez, B., Shen, T., Wu, C., . . . Lee, T. (2012). *Demonstration of scaled Ge p-channel FinFETs integrated on Si*. Paper presented at the Electron Devices Meeting (IEDM), 2012 IEEE International.
- Van, N. H., Muruganathan, M., Kulothungan, J., & Mizuta, H. (2018). Fabrication of a three-terminal graphene nanoelectromechanical switch using two-dimensional materials. *Nanoscale*.
- Walke, A. M., & Mohapatra, N. R. (2012). Effects of Small Geometries on the Performance of Gate First High- κ Metal Gate NMOS Transistors. *IEEE Transactions on Electron Devices*, 59(10), 2582-2588.
- Wei, Q., Xiong, F., Tan, S., Huang, L., Lan, E. H., Dunn, B., & Mai, L. (2017). Porous one-dimensional nanomaterials: design, fabrication and applications in electrochemical energy storage. *Advanced Materials*, 29(20), 1602300.
- Weste, N., & Harris, D. (2010). Datapath subsystems, in CMOS VLSI Design: A Circuits and Systems Perspective: Readington: Addison-Wesley.
- Xie, Q., Xu, J., & Taur, Y. (2012). Review and critique of analytic models of MOSFET short-channel effects in subthreshold. *IEEE Transactions on Electron Devices*, 59(6), 1569-1579.
- Yang, M. (2018). *Characterization of Gate-all-Around Field Effect Transistors Based on BSIM-CMG Model*. Illinois Institute of Technology.
- Yaroshevich, E., & Mileiko, A. (2018). Chemical Elements Used in Engineering.
- Yeh, M.-S., Luo, G.-L., Hou, F.-J., Sung, P.-J., Wang, C.-J., Su, C.-J., Chao, T.-S. (2018). *Ge FinFET CMOS Inverters with Improved Channel Surface Roughness by Using In-situ ALD Digital O₃ Treatment*. Paper presented at the 2018 IEEE 2nd Electron Devices Technology and Manufacturing Conference (EDTM).